Distribution of Time Division.
Multiplexed Data Through Packet
Connections
by: Robert Gordon Dyke
Attorney Docket: N2001-700010

1

External Timing Source(s)

Synchronizer B 5B

2B

Circuit Board N

Time Slot Interchanger

Local TDM Bus

Timing Bus A: Clock, Frame 4A

Timing Bus B: Clock, Frame 4B

1

2A

Circuit Board 1

TIMESLOT INTERCHANGER 3

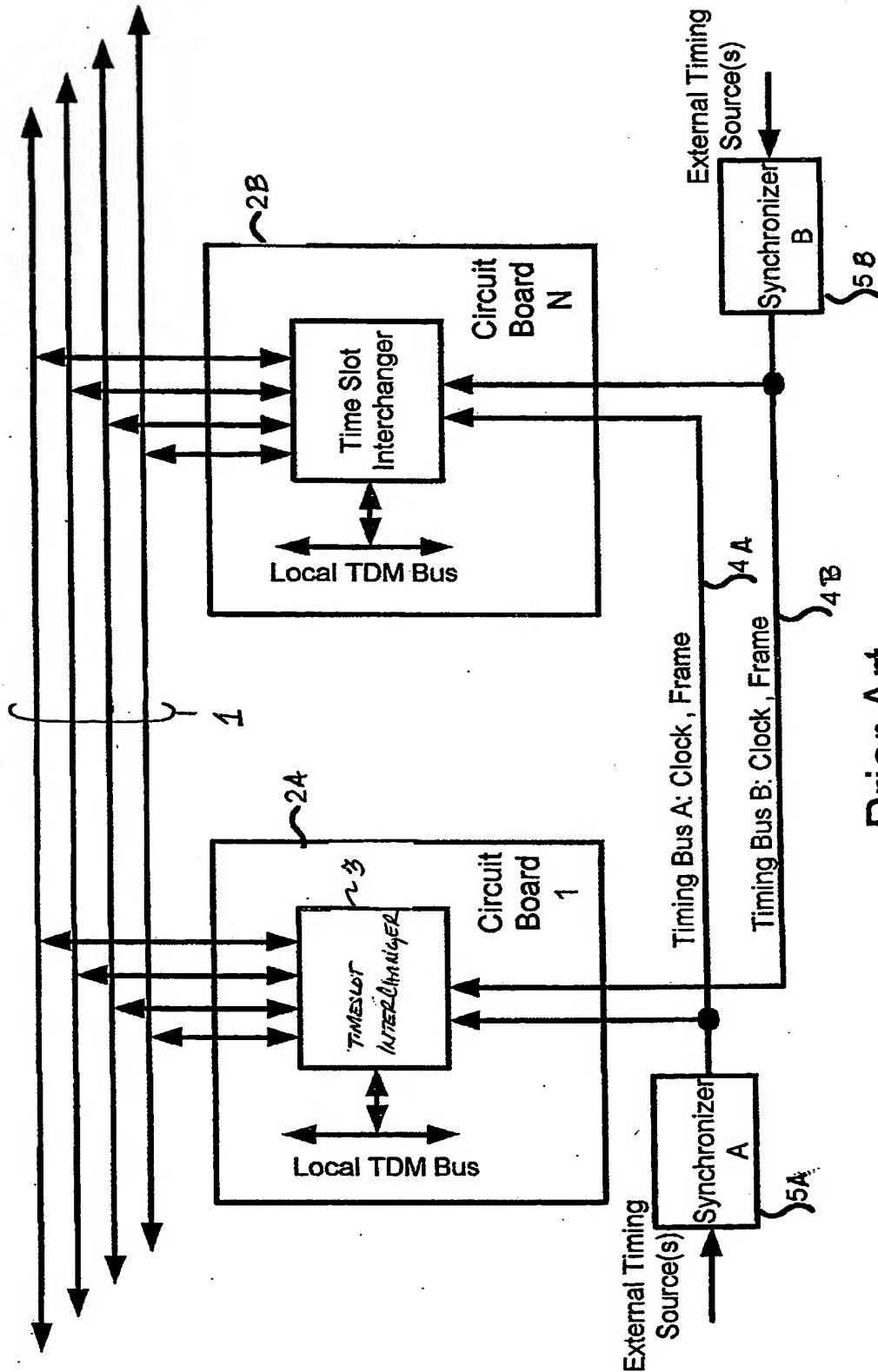Local TDM Bus

Synchronizer A 5A

External Timing Source(s)

Prior Art

Fig. 1

Distribution of Time Division
Multiplexed Data Through Packet
Connections
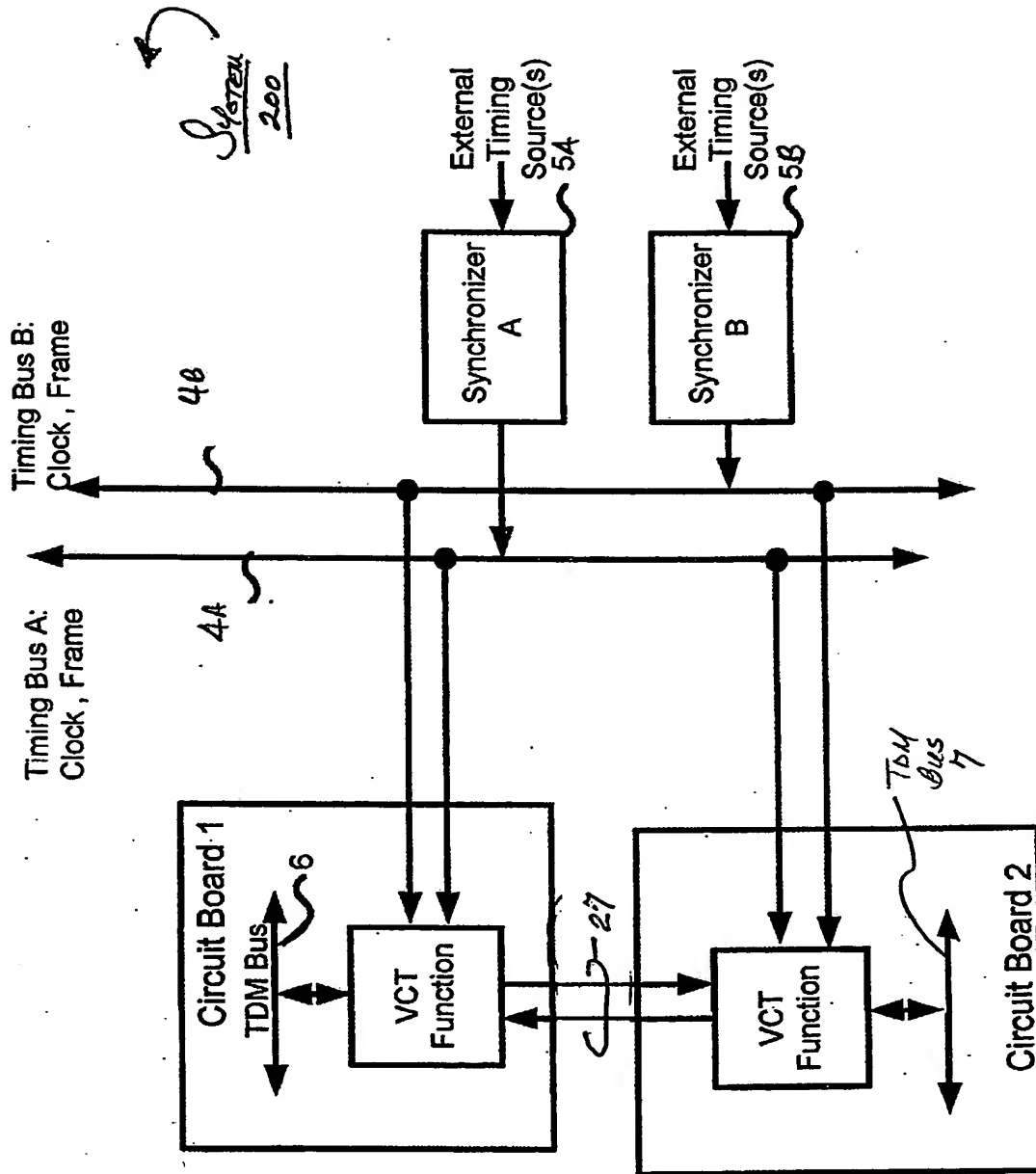by: Robert Gordon Dyke
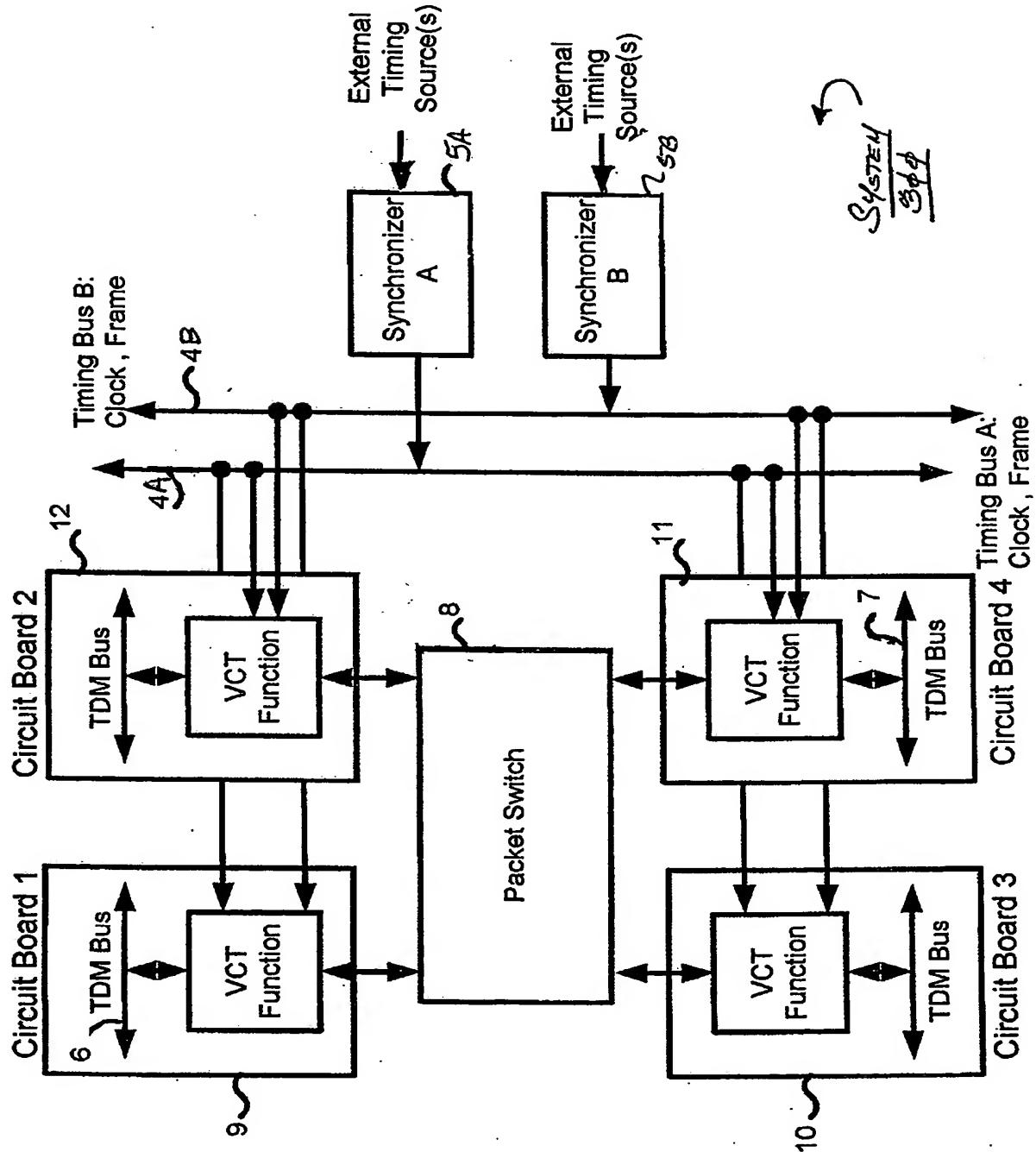Attorney Docket: N2001-700010

2

Fig. 2

Distribution of Time Division
Multiplexed Data Through Packet
Connections
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3

Fig. 3

Distribution of Time Division
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4

Fig. 4

Distribution of Time Division
Multiplexed Data Through Packet
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5

External Timing Source(s)
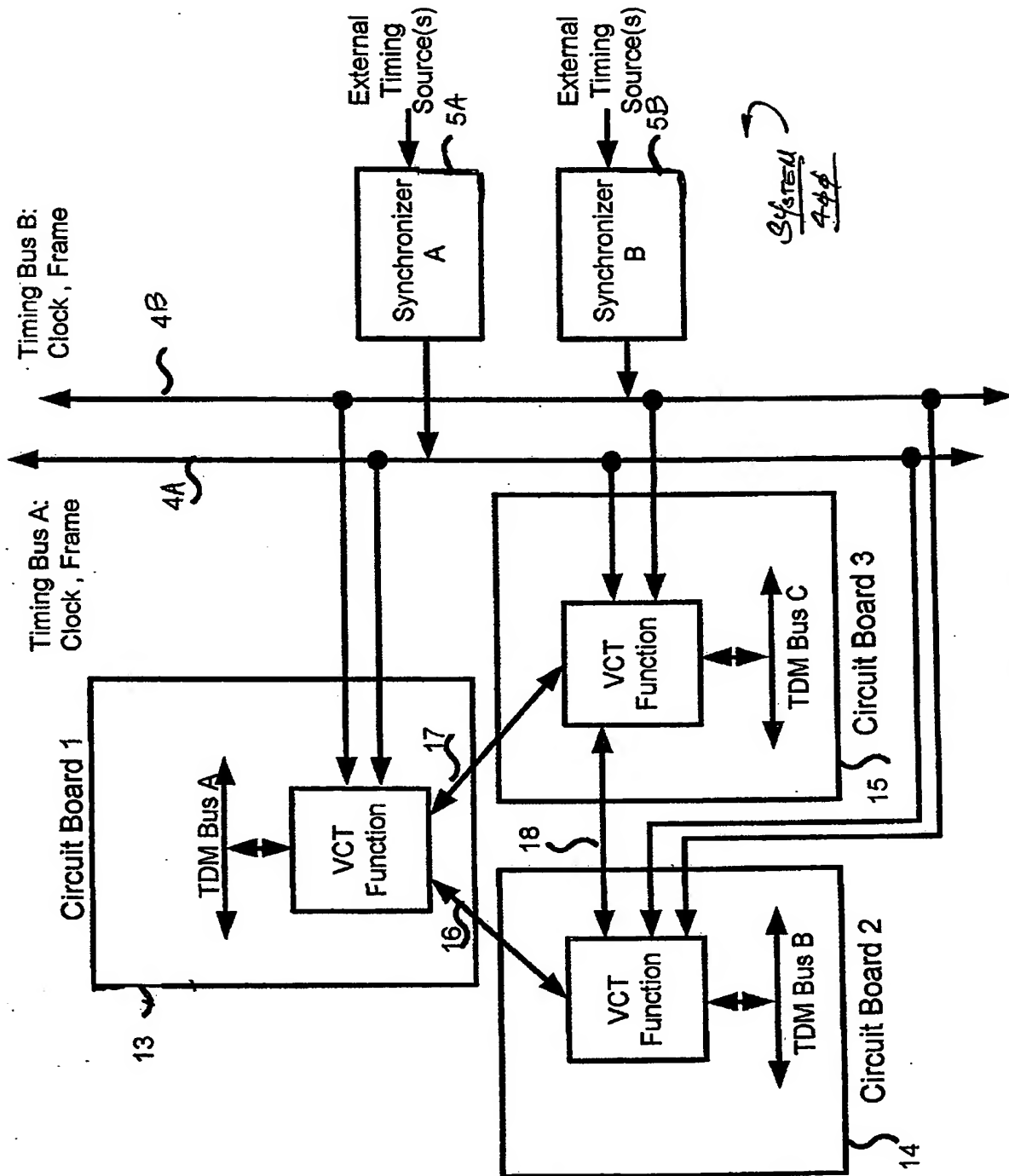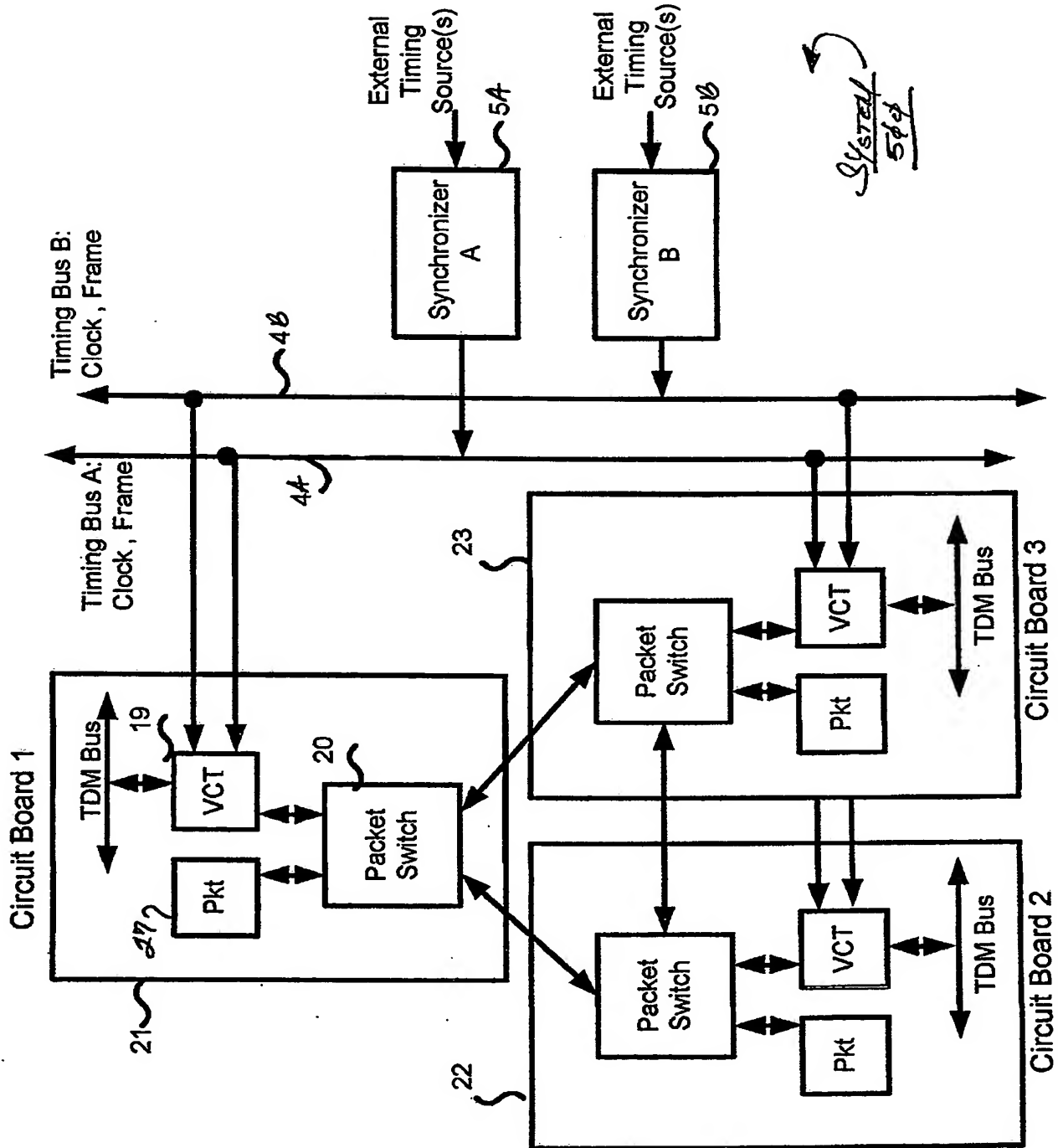External Timing Source(s)

5A

5B

Synchronizer A

Synchronizer B

System 5pt

Timing Bus B: Clock , Frame

Timing Bus A: Clock , Frame

4B

4A

Circuit Board 1

TDM Bus

19

VCT

20

Pkt

27

Packet Switch

21

Circuit Board 3

23

Packet Switch

VCT

TDM Bus

Pkt

Circuit Board 2

Packet Switch

VCT

TDM Bus

Pkt

22

Fig. 5

6

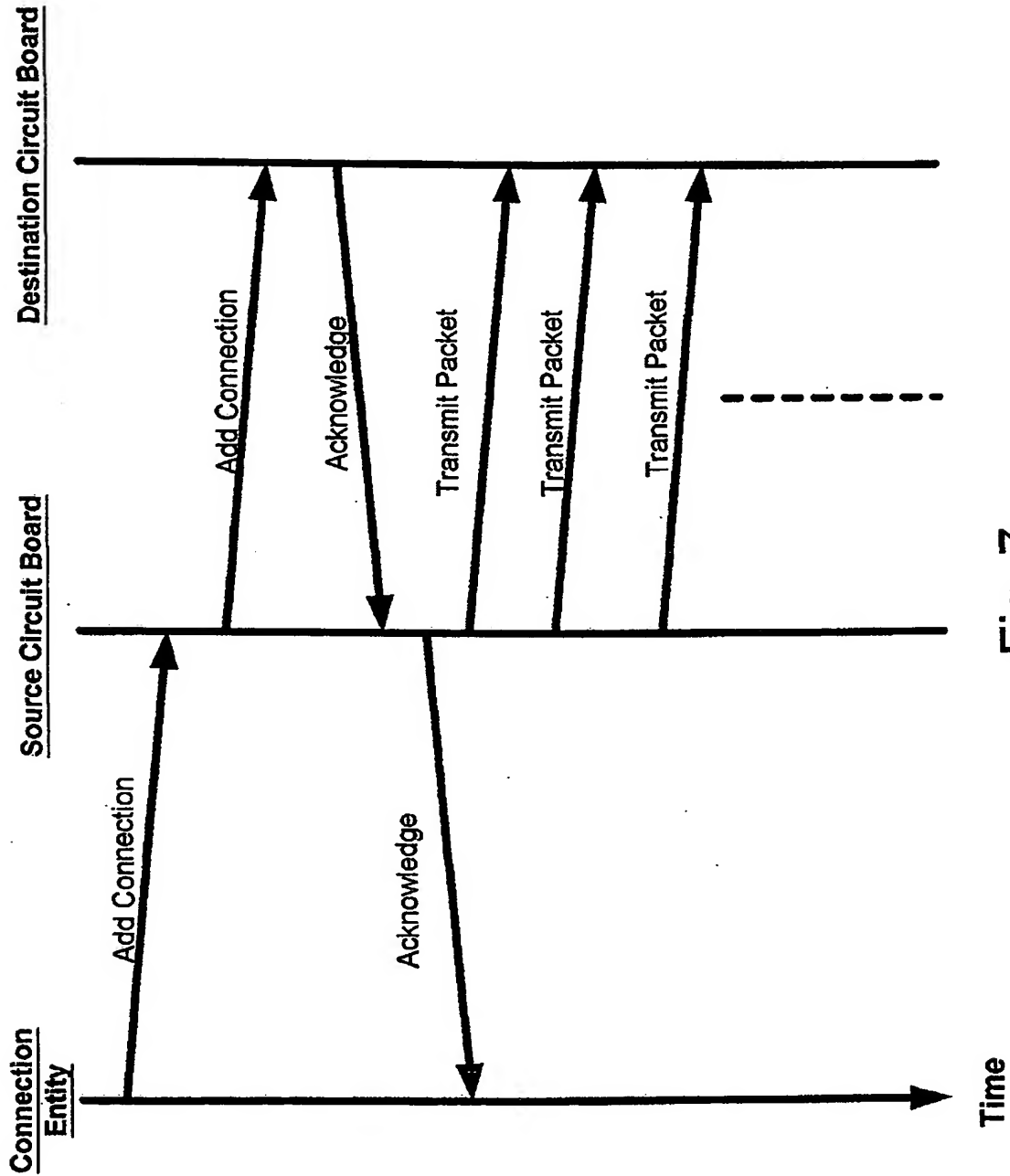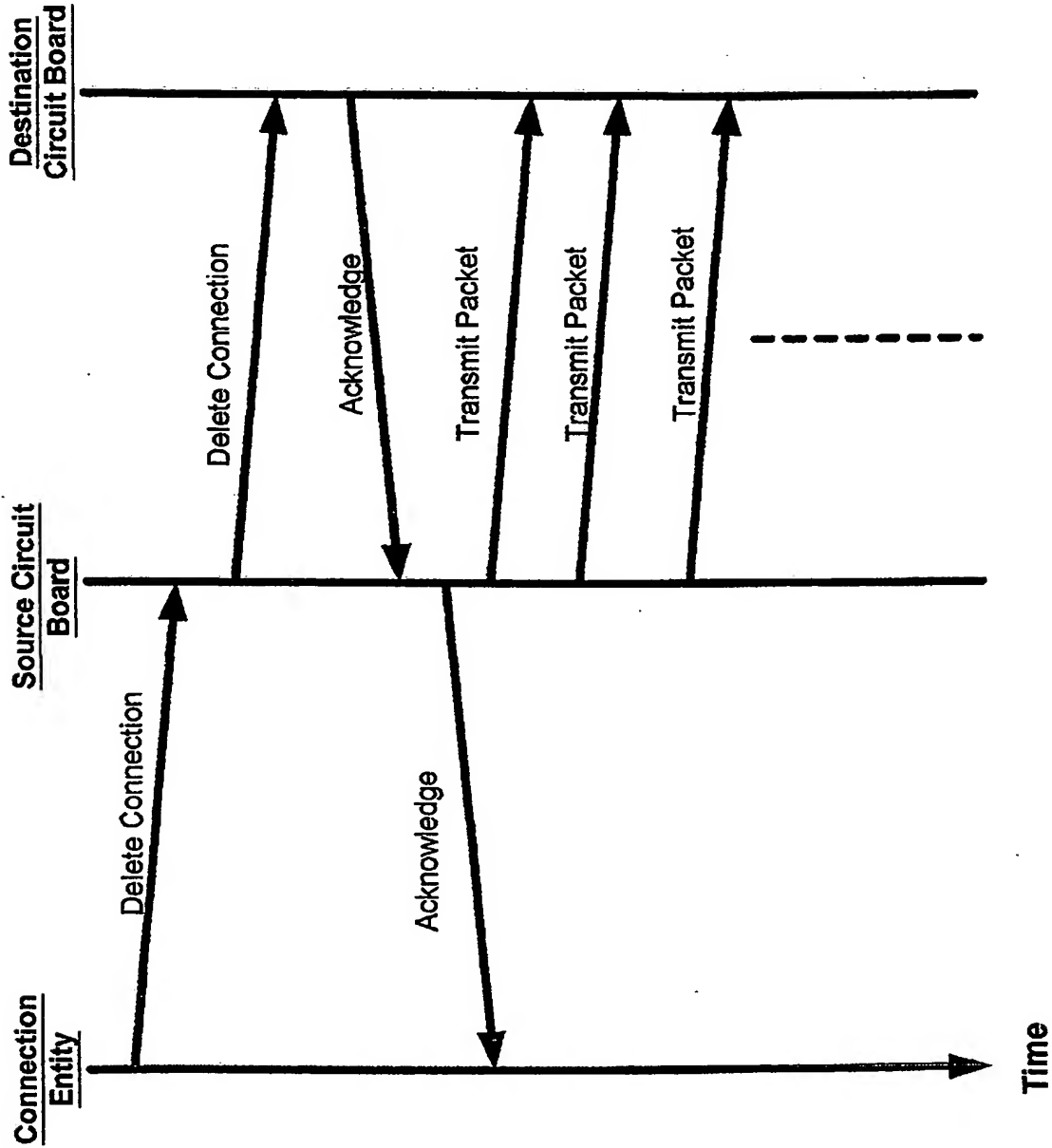| Frame N (125 us)	Frame N +1 (125 us)	Frame N +2 (125 us)	Frame N +3 (125 us)	Frame N +4 (125 us)	Frame N +5 (125 us)
Source creates Frame N packets.	Source xmits Frame N packets.	Destination receives Frame N packets.	Destination arranges Frame N packets in memory.	Destination outputs Frame N packets on local TDM busses.	
	Source creates Frame N+1 packets.	Source xmits Frame N+1 packets.	Destination receives Frame N+1 packets.	Destination arranges Frame N+1 packets in memory.	Destination outputs Frame N+1 packets on local TDM busses.

Fig. 6

Distribution of Time Division
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7

Fig. 7

Distribution of Time Division
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8

Destination Circuit Board

Delete Connection

Acknowledge

Transmit Packet

Transmit Packet

Transmit Packet

Source Circuit Board

Delete Connection

Acknowledge

Connection Entity

Time

Fig. 8

Distribution of Time Division
Multiplexed Data Through Packet
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9

External Timing Source(s)

External Timing Source(s)

Synchronizer A

Synchronizer B

5

5

Timing Bus B: Clock , Frame

Timing Bus A: Clock , Frame

Chassis B

Chassis D

Chassis A

Chassis C

Packet Switch

Uplink(s)

Uplink(s)

Uplink(s)

Uplink(s)

24

25

26

Fig. 9